IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A method for forming a programmable logic array, comprising:

forming a first logic plane that receives a number of input signals, wherein forming the first logic plane includes forming a number of logic cells arranged in rows and columns that are interconnected to provide a number of logical outputs;

forming a second logic plane, wherein forming the second logic plane includes forming a number of logic cells arranged in rows and columns that receive the outputs of the first logic plane and that are interconnected to produce a number of logical outputs such that the programmable logic array implements a logical function; and

wherein forming each of the logic cells includes;

forming a first source/drain region and a second source/drain region separated by a channel region in a substrate;

forming a polysilicon floating gate opposing the channel region and separated therefrom by a gate oxide, the floating gate having a metal layer;

forming a control gate opposing the floating gate; and

forming a low tunnel barrier intergate insulator to separate the control gate from the floating gate, the low tunnel barrier intergate insulator in contact with the metal layer of the floating gate.

2. (Original) The method of claim 1, wherein forming the low tunnel barrier intergate insulator includes forming a metal oxide insulator selected from the group consisting of lead oxide (PbO) and aluminum oxide (Al_2O_3).

3. (Original) The method of claim 1, wherein forming the low tunnel barrier intergate insulator includes forming a transition metal oxide insulator.

4. (Original) The method of claim 3, wherein forming the transition metal oxide insulator includes forming the transition metal oxide insulator selected from the group consisting of Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

5. (Canceled)

6. (Currently Amended) The method of claim [[5]] 1, wherein forming the control gate includes a forming a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

7. (Original) The method of claim 1, wherein forming the first logic plane and the second logic plane each comprise forming NOR planes.

8. (Currently Amended) A method for forming an in service programmable logic array, comprising:

forming a plurality of input lines for receiving an input signal;

forming a plurality of output lines; and

forming one or more arrays having a first logic plane and a second logic plane connected between the input lines and the output lines, wherein forming the first logic plane and the second logic plane forming a plurality of logic cells arranged in rows and columns for providing a sum-of-products term on the output lines responsive to the received input signal, wherein forming each logic cell includes forming a vertical non-volatile memory cell including:

forming a vertical pillar extending outwardly from a semiconductor substrate at intersections of the input lines and interconnect lines and at the intersections of the interconnect lines and the output lines, wherein each pillar includes a first source/drain region, a body region, and a second source/drain region;

forming a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide;

forming a number of polysilicon control gates opposing the floating gates, the control gates having a metal layer; [[and]]

forming a low tunnel barrier intergate insulator to separate the control gate from the floating gate, the low tunnel barrier intergate insulator in contact with metal layer of the control gate; and

forming a number of buried source lines formed of single crystalline semiconductor material and disposed below the pillars in the array for interconnecting with the first source/drain regions of column adjacent pillars in the array.

9. (Original) The electronic system of claim 8, wherein forming the low tunnel barrier intergate insulator includes forming a metal oxide insulator selected from the group consisting of PbO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

10. (Original) The electronic system of claim 8, wherein forming each floating gate includes forming a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

11. (Canceled)

12. (Original) The electronic system of claim 8, wherein forming each floating gate includes forming a vertical floating gate formed in a trench below a top surface of each pillar such that each trench houses a pair of floating gates opposing the body regions in adjacent pillars on opposing sides of the trench.

13. (Original) The electronic system of claim 12, wherein forming the number of control gates includes forming the control gates in the trench below the top surface of the pillar and between the pair of floating gates, wherein each pair of floating gates shares a single control gate line, and wherein each floating gate includes a vertically oriented floating gate having a vertical length of less than 100 nanometers.

14. (Original) The electronic system of claim 12, wherein forming the number of control gates includes forming the control gates in the trench below the top surface of the pillar and between the pair of floating gates such that each trench houses a pair of control gates each addressing the floating gates one on opposing sides of the trench respectively, and wherein the pair of control gates are separated by an insulator layer.

15. (Original) The electronic system of claim 12, wherein forming the number of control gates includes forming the control gates disposed vertically above the floating gates, and wherein each pair of floating gates shares a single control gate.

16. (Original) The electronic system of claim 12, wherein forming the number of control gates includes forming the control gates disposed vertically above the floating gates, and wherein each one of the pair of floating gates is addressed by an independent one of the number of control gates.

17. (Original) The electronic system of claim 8, wherein forming each floating gate includes forming a horizontally oriented floating gate formed in a trench below a top surface of each pillar such that each trench houses a floating gate opposing the body regions in adjacent pillars on opposing sides of the trench, and wherein each horizontally oriented floating gate has a vertical length of less than 100 nanometers opposing the body region of the pillars.

18. (Original) The electronic system of claim 17, wherein forming the number of control gates includes forming the control gates disposed vertically above the floating gates.

19. (Original) A method for operating an in-server programmable logic array, comprising:

writing to one or more floating gates of a number of non-volatile memory cells in one or more arrays using channel hot electron injection, the one or more arrays having a first logic plane and a second logic plane connected between a number of input lines and a number of output lines, wherein number of non-volatile memory cells in the first logic plane and the second logic plane are arranged in rows and columns for providing a sum-of-products term on the output lines

responsive to the received input signal on the input lines, wherein each non–volatile memory cell includes:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator;

erasing charge from one or more floating gates by tunneling electrons off of the floating gate and onto the control gate.

20. (Original) The method of claim 19, wherein erasing charge from one or more floating gates by tunneling electrons off of the floating gates and onto the control gates further includes:

providing a negative voltage to the substrate of an addressed cell; and

providing a large positive voltage to the control gate of the addressed cell.

21. (Original) The method of claim 19, wherein the method further includes writing to one or more floating gates by tunneling electrons from the control gate to the floating gate in one or more addressed cells.

22. (Original) The method of claim 21, wherein writing to one or more floating gates by tunneling electrons from the control gate to the floating gate in one or more addressed cells further includes:

applying a positive voltage to the substrate of an addressed cell; and

applying a large negative voltage to the control gate of the addressed cell.

23. (Original) The method of claim 19, wherein erasing charge from the floating gate by tunneling electrons off of the floating gate and onto the control gate includes tunneling electrons from the floating gate to the control gate through a low tunnel barrier intergate insulator.

24. (Original) The method of claim 23, wherein tunneling electrons from the floating gate to the control gate through a low tunnel barrier intergate insulator includes tunneling electrons from the floating gate to the control gate through a low tunnel barrier intergate insulator selected from the group consisting of PbO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

25. (Original) The method of claim 23, wherein tunneling electrons from the floating gate to the control gate through a low tunnel barrier intergate insulator includes tunneling electrons from a metal layer formed on the floating gate in contact with the low tunnel barrier intergate insulator to a metal layer formed on the control gate and also in contact with the low tunnel barrier intergate insulator.

26. (Original) A method for operating an in-server programmable logic array, comprising:

writing to one or more floating gates of a number of non-volatile memory cells in one or more arrays using channel hot electron injection, the one or more arrays having a first logic plane and a second logic plane connected between a number of input lines and a number of output lines, wherein number of non-volatile memory cells in the first logic plane and the second logic plane are arranged in rows and columns for providing a sum-of-products term on the output lines responsive to the received input signal on the input lines, wherein each non–volatile memory cell includes:

a number of pillars extending outwardly from a substrate, wherein each pillar includes a first source/drain region, a body region, and a second source/drain region;

a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide;

a number of control gates opposing the floating gates;

a number of buried sourcelines disposed below the number of pillars and coupled to the first source/drain regions along a first selected direction in the array of non–volatile memory cells;

a number of control gate lines formed integrally with the number of control gates along a second selected direction in the array of non–volatile memory cells, wherein the number of control gates lines are separated from the floating gates by a low tunnel barrier intergate insulator; and

a number of bitlines coupled to the second source/drain regions along a third selected direction in the array of non–volatile memory cells; and

erasing charge from the one or more floating gates by tunneling electrons off of the one or more floating gates and onto the number of control gates.

27. (Original) The method of claim 26, wherein erasing charge from the one or more floating gates by tunneling electrons off of the floating gate and onto the number of control gate further includes:

providing a negative voltage to a substrate of one or more non-volatile memory cells; and

providing a large positive voltage to the control gate for the one or more non-volatile memory cells.

28. (Original) The method of claim 27, wherein the method further includes erasing an entire row of non-volatile memory cells by providing a negative voltage to all of the substrates along an entire row of non-volatile memory cells and providing a large positive voltage to all of the control gates along the entire row of non-volatile memory cells.

29. (Original) The method of claim 27, wherein the method further includes erasing an entire block of non-volatile memory cells by providing a negative voltage to all of the substrates along multiple rows of non-volatile memory cells and providing a large positive voltage to all of the control gates along the multiple rows of non-volatile memory cells.

30. (New) A method for forming an in service programmable logic array, comprising:

forming a plurality of input lines for receiving an input signal;

forming a plurality of output lines; and

forming one or more arrays having a first logic plane and a second logic plane connected between the input lines and the output lines, wherein forming the first logic plane and the second logic plane forming a plurality of logic cells arranged in rows and columns for providing a sum-of-products term on the output lines responsive to the received input signal, wherein forming each logic cell includes forming a vertical non-volatile memory cell including:

forming a vertical pillar extending outwardly from a semiconductor substrate at intersections of the input lines and interconnect lines and at the intersections of the interconnect lines and the output lines, wherein each pillar includes a first source/drain region, a body region, and a second source/drain region;

forming a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide;

forming a number of control gates opposing the floating gates;

forming a low tunnel barrier intergate insulator to separate the control gate from the floating gate, wherein forming the low tunnel barrier intergate insulator includes forming a metal oxide insulator selected from the group consisting of PbO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5; and

forming a number of buried source lines formed of single crystalline semiconductor material and disposed below the pillars in the array for interconnecting with the first source/drain regions of column adjacent pillars in the array.

31. (New) A method for forming an in service programmable logic array, comprising:

forming a plurality of input lines for receiving an input signal;

forming a plurality of output lines; and

forming one or more arrays having a first logic plane and a second logic plane connected between the input lines and the output lines, wherein forming the first logic plane and the second logic plane forming a plurality of logic cells arranged in rows and columns for providing a sum-of-products term on the output lines responsive to the received input signal, wherein forming each logic cell includes forming a vertical non-volatile memory cell including:

forming a vertical pillar extending outwardly from a semiconductor substrate at intersections of the input lines and interconnect lines and at the intersections of the interconnect

lines and the output lines, wherein each pillar includes a first source/drain region, a body region, and a second source/drain region;

forming a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide;

forming a number of control gates opposing the floating gates, wherein forming each floating gate includes forming a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator;

forming a low tunnel barrier intergate insulator to separate the control gate from the floating gate; and

forming a number of buried source lines formed of single crystalline semiconductor material and disposed below the pillars in the array for interconnecting with the first source/drain regions of column adjacent pillars in the array.

32. (New) The electronic system of claim 31, wherein forming the low tunnel barrier intergate insulator includes forming a metal oxide insulator selected from the group consisting of PbO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

33. (New) A method for forming an in service programmable logic array, comprising:

forming a plurality of input lines for receiving an input signal;

forming a plurality of output lines; and

forming one or more arrays having a first logic plane and a second logic plane connected between the input lines and the output lines, wherein forming the first logic plane and the second logic plane forming a plurality of logic cells arranged in rows and columns for providing a sum-of-products term on the output lines responsive to the received input signal, wherein forming each logic cell includes forming a vertical non-volatile memory cell including:

forming a vertical pillar extending outwardly from a semiconductor substrate at intersections of the input lines and interconnect lines and at the intersections of the interconnect lines and the output lines, wherein each pillar includes a first source/drain region, a body region, and a second source/drain region;

forming a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide, wherein forming each floating gate includes forming a vertical floating gate formed in a trench below a top surface of each pillar such that each trench houses a pair of floating gates opposing the body regions in adjacent pillars on opposing sides of the trench;

forming a number of control gates opposing the floating gates, wherein forming each floating gate includes forming a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator, wherein forming the number of control gates includes forming the control gates disposed vertically above the floating gates, and wherein each one of the pair of floating gates is addressed by an independent one of the number of control gates;

forming a low tunnel barrier intergate insulator to separate the control gate from the floating gate; and

forming a number of buried source lines formed of single crystalline semiconductor material and disposed below the pillars in the array for interconnecting with the first source/drain regions of column adjacent pillars in the array.